Gagan Gupta

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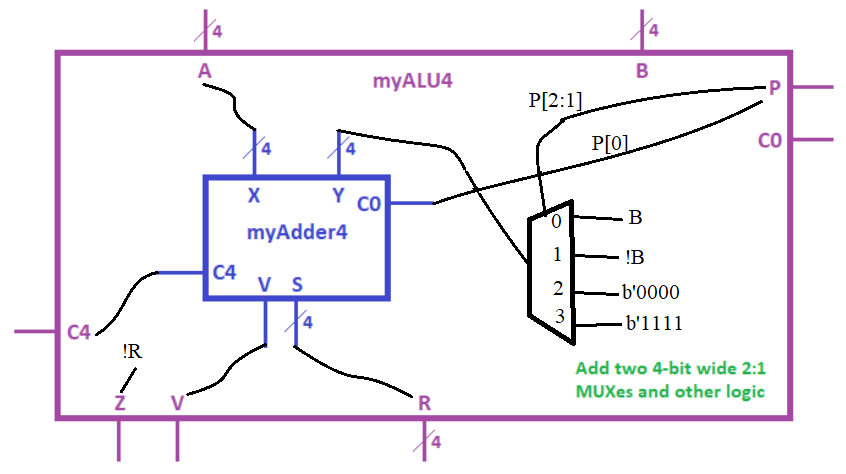
ELEN 21L F 2:15pm

Prelab#6

1. Adder Table

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Op-Select | X | Y | Carry-in | Operation | Note |
| p3p2p1p0 | a3a2a1a0 | b3b2b1b0 |  |  |  |
| 0000 | a3a2a1a0 | b3b2b1b0 | 0 | R=A+B | Add |
| 0001 | a3a2a1a0 | b3b2b1b0 | 1 | R=A+B+1 | Add and Increment |
| 0010 | a3a2a1a0 | b3b2b1b0 | 0 | R=A-B-1 | Subtract and Decrement |
| 0011 | a3a2a1a0 | b3b2b1b0 | 1 | R=A-B | Subtract |

1. Arithmetic Unit Schematic



1. Schematic with operations when p2=1
   1. Above
2. Hierarchical Verilog module

A screenshot of a cell phone

Description automatically generated

* 1. What does p0 control?
     1. The Carry in for the adder
  2. What does p1 control?
     1. The second mux in the chain before the adder
  3. What does p2 control?
     1. The first mux

1. Test plan
   1. Test all 4 rows in the table from number one
   2. Make sure all the outputs are as expected